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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/583,870	05/31/2000	Tominari Nomura	Q59513	1881

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Sughrue Mion Zinn MacPeak & Seas
2100 Pennsylvania Avenue N W
Washington, DC 20037-3202

EXAMINER	
WILLIAMS, LAWRENCE B	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/583,870	NOMURA, TOMINARI	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because:

a.) Examiner suggests applicant delete the word "by" in line 8.

Correction is required. See MPEP § 608.01(b).

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nomura (US Patent 6,272,125 B1) in view of Kakubo et al. (No. Hei 3[1991]-44115.

(1) With regard to claim 1, Nomura discloses in Figs. 1 and 2, a transmitter comprising: average power level calculation circuitry (Fig. 2, (28)) for determining the time-average power of a digital amplitude signal; conversion circuitry (Fig. 1, (6)) for converting the scaled digital

amplitude signal to an analog amplitude signal , and scaling the analog amplitude signal according to a scale factor (second, after d/a conversion) (Fig. 1, (12)) ; and control circuitry (Fig. 1, (20)) for complementarily varying said second scale factors according to said time-average power.

However, Nomura does not disclose conversion circuitry for scaling said digital amplitude signal according to a first scale factor and varying the scale factor according to a time-average power.

However, Kakubo et al. teaches in Fig. 2, conversion circuitry (11A, 11B) for scaling a digital amplitude signal according to a first scale factor, converting the scaled digital amplitude signal to an analog amplitude signal (12A), and scaling the analog amplitude (13A, 13B) signal according to a second scale factor; and control circuitry (15) for complementarily varying the first and second scale factors according to a time-average power.

One skilled in the art would have clearly recognized conversion circuitry for scaling a digital amplitude signal according to a first scale factor, converting the scaled digital amplitude signal to an analog amplitude signal, and scaling the analog amplitude signal according to a second scale factor; and control circuitry for complementarily varying the first and second scale factors according to the time-average power is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Kakubo et al. to modify the invention of Nomura as a method of preventing signal degradation in D/A conversions (pg. 3-4, Problems to be solved by invention).

(2) With regard to claim 2, Nomura also discloses in Figs. 1 and 2, average power level calculation circuitry for determining the a transmitter as claimed in claim 1, wherein the digital amplitude signal is a multiplexed digital amplitude signal in which a plurality of digital spread spectrum signals are multiplexed (col. 1, lines 5-21).

(3) With regard to claim 3, Nomura et al. discloses a transmitter wherein the conversion circuitry is configured to: compare the time-average power of the multiplexed digital amplitude signal with a reference power level and determine a differential power value; and determine a first scale factor (after D/A conversion) according to a differential power value, while Kakubo et al. teaches conversion circuitry is configured to: compare the time-average power of the multiplexed digital amplitude signal with a reference power level and determine a differential power value (before D/A conversion); and determine a first scale factor (after D/A conversion) according to a differential power value. It would be obvious to one skilled in the art to combine the control circuitry as a method of hardware elimination.

(4) With regard to claim 4, Kakubo et al. also discloses in Figs. 2 and 6, wherein the conversion circuitry comprises an interpolator (21A) for interpolating said digital amplitude signal and producing an output signal containing a greater number of bits than a number of bits contained in said digital amplitude signal (pg. 6, line 34- pg. 7, line 3); a bit shifter (2) for selecting a predetermined number of bits from a plurality of bit positions of said output signal of the interpolator, said plurality of bit positions being determined by said first scale factor; a digital-to-analog converter (12A, 12B) for converting the output signal of the interpolator to an analog signal; and a gain-controlled amplifier (23A) for amplifying the analog signal from the digital-to-analog converter at a level determined by a second scale factor.

(5) With regard to claim 5, Nomura also discloses in Fig. 1, a transmitter further comprising: an up-converter for modulating said analog amplitude signal onto a carrier (10); a power amplifier for amplifying the modulated carrier (13); and detection circuitry (15) for detecting power variation of said power amplifier, wherein said control circuitry (20) is responsive to the detected power variation for controlling a second scale factor (col. 2, line 43- col. 3, line 36).

(6) With regard to claim 6, Nomura also disclose wherein the average power level calculation circuitry is a channel management unit (col. 3, line 37 - col. 4, line 5).

(7) With regard to claim 15, claim 15 inherits all limitations of claim 1, above, as claim 15 merely discloses the method of operation of the transmitter disclosed in claim 1.

(8) With regard to claim 16, claim 16 inherits all limitations of claims 4 and 15 above.

(9) With regard to claim 17, Nomura also discloses a communications method comprising: modulating said analog amplitude signal onto a carrier (10); amplifying (13) the modulated carrier; detecting power variation (15) of the modulated carrier; and controlling amplification gain of the analog amplitude signals according to the detected power variation (col. 2, line 43- col. 3, line 36).

5. Claims 7- 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nomura (US Patent 6,272,125 B1) 925 A2) in view of Kakubo et al. (No. Hei 3[1991]-44115.

(1) With regard to claim 7, Nomura discloses in Figs. 1 and 2, a spread spectrum transmitter comprising: a multiplexer (4) for multiplexing a plurality of spread spectrum channels to produce a digital amplitude signal; average power level calculation circuitry (Fig. 2,

(28)) for determining the time-average power of a digital amplitude signal; and conversion circuitry for scaling said digital amplitude signal according to a first scale factor, conversion circuitry (Fig. 1, (6)) for converting the scaled digital amplitude signal to an analog amplitude signal , and scaling the analog amplitude signal according to a second scale factor (Fig. 1, (12)) ; and control circuitry (Fig. 1, (20)) for complementarily varying said second scale factors according to said time-average power.

However, Nomura does not disclose conversion circuitry for scaling said digital amplitude signal according to a first scale factor, and varying the first scale factor according to the time-average power.

However, Kakubo et al. teaches in Fig. 2, conversion circuitry (11A, 11B) for scaling a digital amplitude signal according to a first scale factor, converting the scaled digital amplitude signal to an analog amplitude signal (12A), and scaling the analog amplitude (13A, 13B) signal according to a second scale factor; and control circuitry (15) for complementarily varying the first and second scale factors according to the time-average power.

One skilled in the art would have clearly recognized conversion circuitry for scaling a digital amplitude signal according to a first scale factor, converting the scaled digital amplitude signal to an analog amplitude signal, and scaling the analog amplitude signal according to a second scale factor; and control circuitry for complementarily varying the first and second scale factors according to the time-average power is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Kakubo et al. to modify the invention of Nomura as a

method of preventing signal degradation in D/A conversions (pg. 3-4, Problems to be solved by invention).

(2) With regard to claim 8, Nomura et al. discloses a transmitter wherein the conversion circuitry is configured to: compare the time-average power of the multiplexed digital amplitude signal with a reference power level and determine a differential power value; and determine a first scale factor (after D/A conversion) according to a differential power value, while Kakubo et al. teaches conversion circuitry is configured to: compare the time-average power of the multiplexed digital amplitude signal with a reference power level and determine a differential power value (before D/A conversion); and determine a first scale factor (after D/A conversion) according to a differential power value.

(3) With regard to claim 9, Kakubo et al. also discloses in Figs. 2 and 6, wherein the conversion circuitry comprises an interpolator (21A) for interpolating said digital amplitude signal and producing an output signal containing a greater number of bits than a number of bits contained in said digital amplitude signal (pg. 6, line 34- pg. 7, line 3); a bit shifter (2) for selecting a predetermined number of bits from a plurality of bit positions of said output signal of the interpolator, said plurality of bit positions being determined by said first scale factor; a digital-to-analog converter (12A, 12B) for converting the output signal of the interpolator to an analog signal; and a gain-controlled amplifier (23A) for amplifying the analog signal from the digital-to-analog converter at a level determined by a second scale factor.

(4) With regard to claim 10, Nomura also discloses in Fig. 1, a spread spectrum transmitter further comprising: an up-converter for modulating said analog amplitude signal onto a carrier (10); a power amplifier for amplifying the modulated carrier (13); and detection

circuitry (15) for detecting power variation of said power amplifier, wherein said control circuitry (20) is responsive to the detected power variation for controlling a second scale factor (col. 2, line 43- col. 3, line 36).

(5) With regard to claim 11, Nomura also discloses wherein the average power level calculation circuitry is a channel management unit (col. 3, line 37 - col. 4, line 5).

(6) With regard to claim 12, claim 12 inherits all limitations of claim 7, above as claim 12 merely discloses the method of the transmitter as disclosed in claim 7.

(7) With regard to claim 13, claim 13 inherits all limitations of claims 9 and 12 above.

(8) With regard to claim 14, Nomura also discloses in Fig. 1, a communication method, further comprising: modulating said analog amplitude signal onto a carrier (10); amplifying the modulated carrier (13); detecting power variation of the modulated carrier (15); controlling amplification gain of said analog amplitude signals according to the detected power variation (19, 20).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 703-305-6969. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
August 23, 2004

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600